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INTEGRATED CIRCUIT HAVING ORGANIC SEMICONDUCTOR AND ANODIZED GATE DIELECTRIC

Abstract:

Disclosed is a method of making an integrated circuit comprising the steps of providing a substrate; providing a plurality of discrete regions of gate electrode material electrically connected by electrically conductive paths on the substrate; forming an electrically insulating layer on the gate electrode material by anodic oxidation; disconnecting a conductive path to at least one discrete region of gate electrode material; providing a source electrode and a drain electrode adjacent to the insulating layer on the gate electrode material in the discrete region, the source and drain electrodes having a space between them; and providing an organic semiconductor layer adjacent to the insulating layer and in electrical contact with the source and drain electrodes. The substrate is preferably flexible and polymeric.

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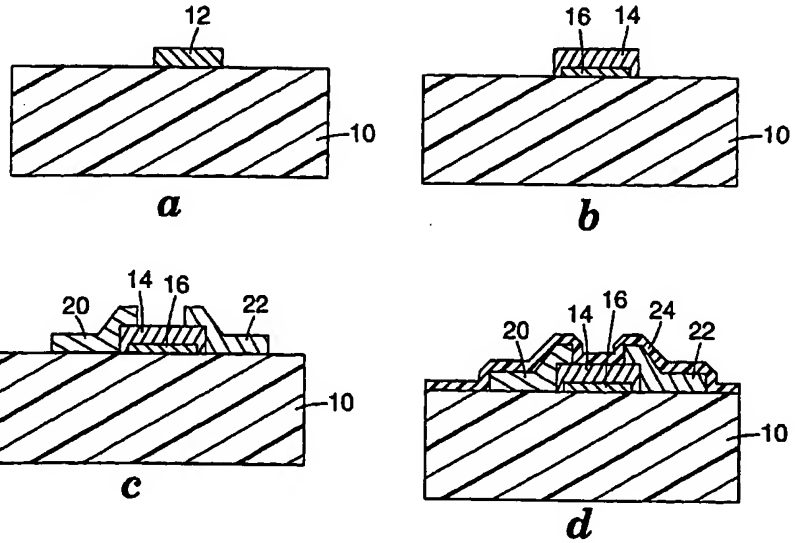

(57) Abstract: Disclosed is a method of making an integrated circuit comprising the steps of providing a substrate; providing a plurality of discrete regions of gate electrode material electrically connected by electrically conductive paths on the substrate; forming an electrically insulating layer on the gate electrode material by anodic oxidation; disconnecting a conductive path to at least one discrete region of gate electrode material; providing a source electrode and a drain electrode adjacent to the insulating layer on the gate electrode material in the discrete region, the source and drain electrodes having a space between them; and providing an organic semiconductor layer adjacent to the insulating layer and in electrical contact with the source and drain electrodes. The substrate is preferably flexible and polymeric.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Integrated Circuit Having Organic Semiconductor and Anodized Gate Dielectric

Technical Field

This invention relates generally to integrated circuits having an organic semiconductor and an anodized gate dielectric and methods of making them. In particular, the present invention relates to methods of producing integrated circuits having organic field effect transistors on a flexible substrate.

Background

Current thin film transistor technology using amorphous or polycrystalline silicon based semiconductors typically uses a glass or quartz substrate upon which the various elements of the transistor circuit are provided. Typically, a gate electrode is first formed on the insulating glass substrate by any well known thin film deposition technique such as sputtering. An insulator, such as silicon nitride, is provided on top of the gate metal and serves as the transistor's gate dielectric. This insulator must be of high quality, having low leakage current, high breakdown field, and being free of pinholes and resistant to charge trapping. It is preferable that the dielectric have a large dielectric constant. To provide these qualities, plasma-enhanced chemical vapor deposition processes are typically employed, using substrate temperatures over 300°C.

Amorphous or polycrystalline silicon is deposited on top of the gate dielectric and patterned, forming a semiconductor channel. It is common practice to heat the substrate above 250°C during the silicon deposition. Finally the source and drain electrodes, separated from each other by the semiconductor channel, are deposited on the insulating layer over the gate electrode.

The substrate must be compatible with the high temperatures required during the formation of a polycrystalline or amorphous silicon based thin film transistor. Reducing the process temperatures, for example during the deposition of the silicon, results in poorer transistor performance. Therefore, the type of substrate must be selected based on the maximum temperature the thin film transistor fabrication process requires to obtain a desired level of device and electrical circuit performance. This constraint precludes the use of many readily available polymer substrates that soften and lose

dimensional stability at temperatures above about 150°C, thereby making it difficult or impossible to do precision alignment of subsequent integrated circuit elements.

Organic thin film field effect transistors (OFETs) have been proposed for applications where low-cost or substrate flexibility is an important feature. For example, see Z. Bhao, "Materials and Fabrication Needs for Low-Cost Organic Transistor Circuits," Advanced Materials, vol. 12, No. 3, pp. 227-230; Feb. 3, 2000. Organic semiconductors can be used to create thin film transistors and integrated circuits. Moreover, the maximum temperatures required to deposit organic semiconductors suitable for use in transistors are typically less than 100°C. However, these organic semiconductor transistors still require a high-quality gate dielectric—comparable to that used in amorphous-silicon transistors. Furthermore, organic-semiconductor transistors benefit significantly from the use of a gate dielectric with a high dielectric constant, providing higher field-effect mobility at lower gate voltage (see C.D. Dimitrakopoulos, et al., Advanced Materials 11, 1372-1375 (1999)).

Laboratory demonstrations of organic semiconductor transistors have paid little attention to the quality of the gate dielectric, or have used gate dielectrics formed by high-temperature or high-vacuum techniques.

Disclosure of Invention

According to an embodiment of the invention, a method of making an integrated circuit begins with a substrate that is preferably polymeric and flexible. A plurality of discrete regions of gate electrode material, electrically connected by means of electrically conductive paths, is provided on the substrate. An insulating layer then is formed on the gate electrode by anodically oxidizing the gate electrode material. After the anodic oxidation step, the electrically conductive path(s) to at least one discrete gate electrode may be disconnected. A source electrode and a drain electrode then are placed adjacent to the insulating layer of the gate electrode material, with a space between the source electrode and the drain electrode. An organic semiconductor layer physically connects the source and drain electrodes. The voltage applied to the gate

electrode controls the conductivity of the semiconductor channel between the source and drain.

The present invention provides a process suitable for high-volume, low-cost manufacturing of integrated circuits using OFETs on a flexible substrate. The high temperature or high vacuum processes that are typical of conventional semiconductor manufacturing are not necessary with this invention. A high-quality gate dielectric is achieved with the present invention using only low-temperature processes. A flexible polymeric substrate can form the base for the process and allow roll-to-roll or web processing. Such polymeric substrates are highly desirable because they are relatively low cost, lightweight, and resistant to breakage.

This invention eliminates the need for precise alignment techniques between the gate and gate dielectric layers and the associated deleterious effects on process speed and manufacturing yield, thereby enabling continuous or quasi-continuous manufacturing of organic semiconductor integrated circuits. The electrically insulating layer on the gate electrode of the invention has a high dielectric breakdown field, high relative dielectric constant, and low leakage current, which are important to integrated circuit and OFET device operation.

The figures and the detailed description that follow more particularly exemplify certain preferred embodiments using the principles disclosed herein.

Brief Description of the Drawings

Figure 1 is a cross-sectional illustration of a sequence of steps of one embodiment of the present invention.

Detailed Description

Referring now to Figure 1(a), an electrically conducting material in the form of a gate electrode precursor 12 is provided on flexible polymeric substrate 10 in one embodiment of the present invention.

Materials useful for the substrate include inorganic and organic materials. For example, useful materials can include silicon, glass, metal foils that may have an insulating layer, and polymeric materials including polyester and polyimides, which may be flexible.

In one preferred embodiment, the substrate is flexible. This allows for continuous roll processing, providing economy of scale and economy of manufacturing over earlier flat and/or rigid substrates. The flexible substrate chosen preferably is capable of wrapping around the circumference of a cylinder of less than about 30 cm diameter without distorting or breaking. The substrate chosen more preferably is capable of wrapping around the circumference of a cylinder of less than about 10 cm diameter without distorting or breaking the substrate. The substrate chosen most preferably is capable of wrapping around the circumference of a cylinder of less than about 3 cm diameter without distorting or breaking the substrate. The preferred substrate may be rolled upon itself.

In Figure 1(b), electrically insulating layer 14 is provided contiguous to gate electrode 16. The anodized gate portion of the thin film transistor in this view is ready for further processing.

The gate electrode material provided on the substrate can be any useful conductive material that will oxidize to form an insulator having a dielectric breakdown voltage greater than the voltages anticipated to be applied to the transistor of which the gate electrode is an integral part. This material should form a continuous conformal layer over the gate electrode, that is free of cracks and pinholes and allows negligible leakage current between the gate and source or gate and drain electrodes.

Low cost is also a desirable feature in the gate material. Preferred materials include pure metals and alloys, sometimes termed valve metals, including aluminum, titanium, tantalum, zinc, magnesium, niobium, and alloys and multilayers thereof. The gate material preferably is provided on the substrate in a pattern of electrically connected electrodes. Anodization of an appropriate gate material results in a gate dielectric material with extremely low leakage current and high dielectric constant (ε_r), e.g., Al_2O_3 (ε_r ~9.5), TiO_2 (ε_r ~80), or Ta_2O_5 (ε_r ~24), which are highly desirable for organic-semiconductor transistors.

The insulating layer electrically separates the gate from the source and drain electrodes. It comprises an oxide of the gate material, and is formed by oxidizing the gate material, thereby eliminating the need for depositing the insulating layer in a separate step. The insulating layer, or gate dielectric, forms wherever the gate material

is exposed to an anodizing electrolyte. Therefore, the edges or sidewalls of the gate material will anodize along with the top surface, providing excellent and reliable electrical isolation of the gate from the source and drain electrode.

No precise registration is necessary for this anodization step. This can be an important advantage because each patterning step typically increases complexity and adds another opportunity for waste. This technique of anodization enables rapid integrated circuit fabrication. When a plurality of gates is provided on the substrate in a pattern of electrically connected electrodes, current can be supplied to the network, anodically oxidizing a plurality of the gates in one process step, still without the need for precise registration of a mask or other alignment means.

Anodic oxidation of conductive traces in integrated circuit manufacture is known. For example, oxidation can be carried out by using a 3% aqueous solution of tartaric acid that is adjusted to pH 7.0 with ammonia, then diluted ten-fold by ethylene glycol, as described in U. S. Patent No. 5,889,573; by using propylene glycol mixed in a 3:1 solution of a 1% ammonium borate solution or a 3% tartaric acid solution, then adjusting the pH to 6 or 7 with ammonia, as described in Japanese Kokai Publication 10-093105; by using a 10% aqueous ammonium adipate solution, as described in Japanese Kokai Publication 62-094912, Example 1; or by using electrolyte solutions of ammonium tartrate, triammonium citrate, diammonium hydrogen phosphate, or ammonium tetraborate-boric acid, as described by K. Ozawa et al., *J. Electrochem. Soc.*, vol. 141, No. 5, May 1994, pp. 1325-1333. In a typical procedure, the conductive traces to be anodized are immersed in the electrolyte solution and electric current is applied, typically by increasing voltage at constant current.

Electrically conductive paths between gate material regions can be disconnected by any useful means if those paths are not required for the subsequent functioning of the integrated circuit. Preferred processes selectively remove a portion of the conductive network while not substantially harming the gate material with the insulating layer. For example, mechanically abrading, laser ablating, electrical fusing, chemical etching, and plasma etching are useful processes to remove undesired conductive paths between gate electrode regions. Certain methods may be more desirable in some situations, such as selecting non-chemical methods when the substrate is susceptible to chemical attack.

The conductive paths can be removed immediately after the step of forming the insulation layer, or later, such as after the step of providing the source and drain electrodes.

Additionally, the electrical connections between otherwise separate gate electrode regions can be anodized along with the gate material regions. By controlling the volume of the conducting paths in the network, the anodization can be self-limiting. That is, when a sufficient segment of the conductive path to a gate electrode region is anodized, no more current flows and anodic oxidation of the gate electrode connected to the path ceases, thereby providing a reproducible gate dielectric thickness. This may be accomplished, for example, by depositing and patterning the gate material in two steps, so that the conductive paths are thinner than the gate electrodes.

In some applications it can be desirable to maintain electrical connections to one or more gate electrode regions. Selectively removing one or more paths in the conductive network by the techniques described above achieves a desired wiring pattern.

A release coating can be provided on the substrate before the electrically conductive networks between gate electrode regions are provided on the substrate. The release coating preferably is provided in a pattern that excludes the gate electrode regions. After forming the insulating layer, the conductive networks are more easily removed by any useful means, including those described above. A release coating can allow the use of ultrasound or relatively light mechanical abrasion, optionally in concert with an appropriate solvent, to remove the conductive path while not detrimentally affecting the remaining circuit.

Any suitable release coating can be used. The release coating is preferably easily coated on the substrate and preferably does not substantially inhibit the process chosen to provide the gate material regions or the conductive network. Such release coatings include, for example, photoresists, fluoropolymers, inorganic thin films, and silicones. The release coating may be patterned by known techniques, including photolithography or ink jet printing.

At least one electrode is then provided contiguous to insulating layer 14. As shown in Figure 1(c), source electrode 20 and drain electrode 22 are provided contiguous to insulating layer 14 and spaced apart.

The source electrode and the drain electrode are located near the gate electrode with a space between them. The source and drain electrodes are adjacent to the insulating layer that has been formed on the gate electrode. These thin film electrodes can be provided by any useful means such as physical vapor deposition (e.g., thermal evaporation, sputtering) or ink jet printing. The patterning of these electrodes can be accomplished by known methods such as shadow masking, additive photolithography, subtractive photolithography, printing, and pattern coating.

In Figure 1(d), organic semiconductor layer 24 is provided contiguous to insulating layer 14, source electrode 20, and drain electrode 22, such that voltage provided in gate electrode 16 electrically controls the conductivity of the organic semiconductor between source electrode 20 and drain electrode 22.

One useful material for this organic semiconductor layer is pentacene. Other useful organic semiconductors include anthracene, tetracene, napthalene, perylene, copper phthalocyanine, oligothiophenes, and tetracyanoquinodimethane (TCNQ). The organic semiconductor layer can be provided by any useful method, such as, for example, physical vapor deposition, spin coating, and printing techniques.

The entire process of making the thin film transistor can be carried out below about 200°C, more preferably below about 175°C, most preferably below about 120°C. These temperatures are well below traditional integrated circuit and semiconductor processing temperatures, which enables the use of any of a variety of relatively inexpensive flexible polymeric substrates. This enables production of relatively inexpensive integrated circuits containing OFETs.

For clarity and consistency, the transistors described above are all described with the source and drain electrodes deposited directly on the gate dielectric before the organic semiconductor is deposited on the gate dielectric between the source and drain electrodes. It is also within the scope of the present invention that such devices can be made by depositing the organic semiconductor before depositing the source and drain electrodes.

The processes of the present invention can be performed while the substrate is itself a web or the substrate is provided on a moving carrier web suitable for roll-to-roll manufacturing. Such roll-to-roll processes are known in other fields. The economies of

scale involved with moving web processes are achieved with the present invention, making the integrated circuits of the invention relatively inexpensive.

Various modifications and alterations of this invention will become apparent to those skilled in the art without departing from the scope and principles of this invention, and it should be understood that this invention is not to be unduly limited to the illustrative embodiments set forth hereinabove.

Claims

1. A method of making an integrated circuit comprising the steps of:

a) providing a substrate;

b) providing a plurality of discrete regions of gate electrode material electrically connected by electrically conductive paths on the substrate;

c) forming an electrically insulating layer on the gate electrode material by anodic oxidation;

d) disconnecting a conductive path to at least one discrete region of gate electrode material;

e) providing a source electrode and a drain electrode adjacent to the insulating layer on the gate electrode material in the discrete region, the source and drain electrodes having a space between them;

f) providing an organic semiconductor layer adjacent to the insulating layer and in electrical contact with the source and drain electrodes.

2. The method of claim 1 further comprising the steps of:

i) providing, before step (b), a release coating on at least a portion of a surface of the substrate;

ii) carrying out step (b) such that the gate electrode material is deposited on a surface of the substrate in regions substantially free of release coating; and

iii) removing at least some electrically conductive paths between gate electrode material from the release coated regions of the surface after step (c).

3. The method of claim 1 or 2 wherein the plurality of electrically connected discrete regions of gate electrode material include conductive paths comprising an oxidizable material having a predetermined volume such that the step of forming the insulating layer also oxidizes the conductive paths so as to electrically disconnect at least one conductive path to a discrete gate electrode material region.

4. The method of claim 1, 2 or 3 wherein the step of disconnecting the conductive paths further comprises a step selected from mechanically abrading, laser ablating, electrical fusing, chemical etching, and plasma etching.

5. A method of making an integrated circuit comprising the steps of:

a) providing a substrate;

b) providing a plurality of discrete regions of gate electrode material electrically connected by electrically conductive paths on the substrate;

c) forming an electrically insulating layer on the gate electrode material by anodically oxidizing the gate electrode material and the conductive paths therebetween, such that the electrical network to a discrete region is electrically disconnected upon oxidation of the conductive path material to said discrete region.

6. The method of claim 5 further comprising the steps of:

d) providing a source electrode and a drain electrode contiguous to the insulating layer of the gate electrode material, the source and drain electrodes having a space between them; and

e) providing an organic semiconductor layer selectively electrically connecting the electrodes in a circuit.

7. The method of any of the above claims wherein the substrate is flexible.

8. The method of any of the above claims wherein the substrate is polymeric.

9. The method of any of the above claims wherein at least one of the electrodes is provided by a technique selected from additive photolithography, subtractive photolithography, shadow masking, printing, and pattern coating.

10. The method of any of the above claims carried out in its entirety below a peak temperature of 200°C.

11. The method of any of the above claims carried out on a web.

12. The method of any of the above claims wherein the gate electrode material is selected from the group comprising aluminum, tantalum, titanium, zinc, magnesium, niobium, and alloys and multilayers thereof.

13. An integrated circuit made by the method of any of the above claims.

14. An integrated circuit comprising:

a flexible polymeric substrate;

two or more anodized gate electrodes on the substrate;

at least partially anodized electrical pathways connecting the anodized gate electrodes, wherein the pathways comprise a material used in the gate electrode;

a source electrode and a drain electrode contiguous to each anodized gate electrode, the source and drain electrodes having a space between them; and

an organic semiconductor layer contiguous to the anodized gate electrodes selectively electrically connecting the source and drain electrodes.

15. The integrated circuit of claim 14 wherein the at least partially anodized pathways electrically connect at least two of the anodized gate electrodes.

16. The integrated circuit of claim 14 or 15 further comprising a plurality of anodized gate electrodes.

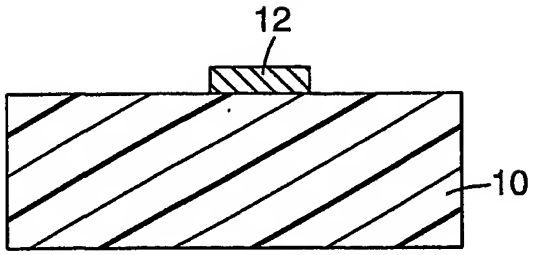

Fig. 1a

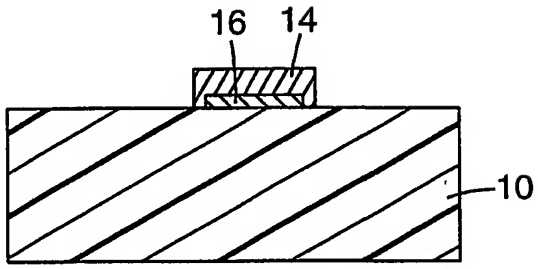

Fig. 1b

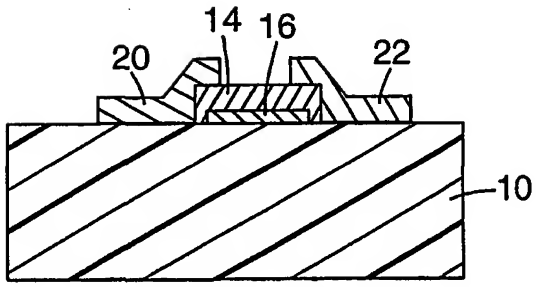

Fig. 1c

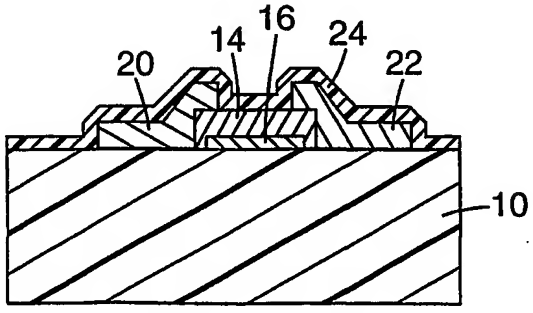

Fig. 1d

INTERNATIONAL SEARCH REPORT

Inte ial Application No
PC1/US 01/00925

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TATE J ET AL: "Anodization and microcontact printing on electroless silver: solution-based fabrication procedures for low-voltage electronic systems with organic active components" LANGMUIR, 11 JULY 2000, AMERICAN CHEM. SOC, USA, vol. 16, no. 14, pages 6054-6060, XP002173931 ISSN: 0743-7463 the whole document --- -/--	1,5,13, 14

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
3 August 2001	17/08/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Königstein, C

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INTERNATIONAL SEARCH REPORT

Inte[illegible]al Application No
PC.. .. 01/00925

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	OZAWA K ET AL: "ANODIC OXIDE FILMS AS A GATE DIELECTRIC FOR A THIN FILM TRANSISTOR" JOURNAL OF THE ELECTROCHEMICAL SOCIETY, ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, US, vol. 141, no. 5, 1 May 1994 (1994-05-01), pages 1325-1333, XP000470153 ISSN: 0013-4651 cited in the application the whole document ---	
A	DIMITRAKOPOULOS C D ET AL: "LOW-VOLTAGE, HIGH-MOBILITY PENTACENE TRANSISTORS WITH SOLUTION- PROCESSED HIGH DIELECTRIC CONSTANT INSULATORS" ADVANCED MATERIALS, VCH VERLAGSGESELLSCHAFT, WEINHEIM, DE, vol. 11, no. 16, 10 November 1999 (1999-11-10), pages 1372-1375, XP000875157 ISSN: 0935-9648 cited in the application the whole document -----	